In The Claims:

1. (Currently Amended) A graphics processing apparatus comprising:

an input mechanism;

a control mechanism configured to receive one or more items of data from said input mechanism;

one or more pipelines configured to receive said items of data as instructed by said control mechanism; and

one or more graphics processing units coupled to said pipelines configured to perform one or more computations on said items of data, said one or more graphics processing units owning a portion of screen area dependent on a number of graphics that are enabled.

2. (Original) The graphics processing apparatus of claim 1 wherein said control mechanism is a mode bit.

3. (Original) The graphics processing apparatus of claim 1 wherein said items of data comprise pixels.

4. (Original) The graphics processing apparatus of claim 1 wherein said control mechanism is configured to use all of said pipelines, thereby simulating a high-end chip.

5. (Original) The graphics processing apparatus of claim 1 wherein said control mechanism is configured to use a subset of said pipelines, thereby simulating a low-end chip.

6. (Original) The graphics processing apparatus of claim 1 wherein said graphics processing unit comprises:

a raster color unit, a texture address unit, and a scan unit coupled to one of said pipelines;

a pixel shader coupled to said texture address unit and said raster color unit; and

a frame buffer coupled to said pixel shader, wherein said graphics processing unit is configured to process one or more pixels.

7. (Currently Amended) A method for selectably configuring a graphics processing apparatus comprising:

using an input mechanism to provide one or more items of data to one or more pipelines;

routing said items of data to some or all of said pipelines with a control mechanism; and

operating on said items of data in one or more graphics processing units coupled to said pipelines;

assigning a portion of screen ownership to each of said graphics processing units dependent on a number of enabled graphics processing units.

8. (Original) The method of claim 7 wherein said control mechanism is a mode bit.

9. (Original) The method of claim 7 wherein said items of data comprise pixels.

10. (Original) The method of claim 7 wherein said control mechanism is configured to use all of said pipelines, thereby simulating a high-end chip.

11. (Original) The method of claim 7 wherein said control mechanism is configured to use a subset of said pipelines, thereby simulating a low-end chip.

12. (Original) The method of claim 7 wherein said graphics processing unit comprises:

a raster color unit, a texture address unit, and a scan unit coupled to one of said pipelines;

a pixel shader coupled to said texture address unit and said raster color unit; and

a frame buffer coupled to said pixel shader, wherein said graphics processing unit is configured to process one or more pixels.

13. (Currently Amended) A computer program product comprising:

a computer usable medium having computer readable program code embodied therein configured to selectably configure a graphics processing apparatus, said computer program product comprising:

computer readable code configured to cause a computer to use an input mechanism to provide one or more items of data to one or more pipelines;

computer readable code configured to cause a computer to route said items of data to some or all of said pipelines with a control mechanism; and

computer readable code configured to cause a computer to operate on said items of data in one or more graphics processing units coupled to said pipelines;

computer readable code configured to cause a computer to assign a portion of screen ownership to each graphics processing unit depending on a number of enabled graphics processing units.

14. (Original) The computer program product of claim 13 wherein said control mechanism is a mode bit.

15. (Original) The computer program product of claim 13 wherein said items of data comprise pixels.

16. (Original) The computer program product of claim 13 wherein said control mechanism is configured to use all of said pipelines, thereby simulating a high-end chip.

17. (Original) The computer program product method of claim 13 wherein said control mechanism is configured to use a subset of said pipelines, thereby simulating a low-end chip.

18. (Original) The computer program product of claim 13 wherein said graphics processing unit comprises:

a raster color unit, a texture address unit, and a scan unit coupled to one of said pipelines;

a pixel shader coupled to said texture address unit and said raster color unit; and

a frame buffer coupled to said pixel shader, wherein said graphics processing unit is configured to process one or more pixels.

19. (Currently Amended) A method of producing a processing apparatus comprising:

producing a processing apparatus having a full set of features;

including in said processing apparatus a mechanism for disabling a subset of said full set of features and assigning screen ownership based on the state of enablement of said features.

20. (Original) The method of claim 19 wherein a processing apparatus having said full set of features enabled is distributed for a first price and a processing apparatus having said subset of said full set of features disabled is distributed for a second price.

21. (Original) The method of claim 20 wherein said first price is higher than said second price.

22. (Original) The method of claim 19 wherein said mechanism permanently disables said subset of said full set of features.

23. (Original) The method of claim 19 further including a plurality of mechanisms for disabling a plurality of subsets of features of said full set of features.